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ORIGINAL PAPER

Optoelectronic properties of porous silicon heterojunction photodetector

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Abstract: In this paper, formation of a nano-crystaline porous silicon layer on *n*-type and *P*-type crystalline Si substrates prepared by the electrochemical etching and photo-electrochemical etching techniques (in order to fabricate heterojunctions photodetector) has been studied. The fabricated Al/PS/n-Si/Al photodetector has responsivity to white light higher than that for Al/PS/p-Si/Al photodetector. The values of minority carrier life time obtained are 125 and 208 μs for junctions made on *n*-type silicon substrates at etching time of 5 and 10 min respectively. While, junctions made on *p*-type silicon substrates prepared at the same etching time have life time of 83–113 μs.

Keywords: Nano-structure; Porous silicon; Electrochemical etching; OCVD; Heterojunction; Minority carrier life time

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1. Introduction

Nanomaterials have gained a special attention in development of many electronic devices [1–5]. For example, porous silicon (pS) has been widely used in many applications such as light emitting diodes and solar cells [6]. Electrochemical etching is one of the simplest and most reliable method used to synthesis pS [7]. A widely used method for carrier life time estimation is open circuit voltage decay (OCVD) because of its straight forward interpretation and simple structure test involved in these measurements [8]. Minority carrier life time is a fundamental parameter for today's semiconductor industry, since it influences dramatically photovoltaic performances of many devices, such as silicon-on-insulator (SOI), power devices, photodetectors and solar cells. Besides, it is one of the very few parameters that gives information about surface defect densities [9]. OCVD method is one of the most widespread methods for determining carrier lifetime in bulk of diode structures. When forward current flows through diode, circuit is abruptly open and forward voltage drop decay is measured. For particular case of a thick diode structure with a homogeneous base and abrupt PN junction, carrier life time can be determined from slope of voltage decay [10] by using the following relation:

$$\tau = m\frac{KT}{q}\left(\frac{dV}{dt}\right)^{-1} \quad (1)$$

where conditions, $1 \leq m \leq 2$ $m = 1$ describes low injection $m = 2$ should be used under high injection conditions), k is Boltzmann constant, T absolute temperature and q elementary charge. This approximation expresses the so-called "OCVD carrier lifetime". Generally, exact solution can be obtained by solving continuity equation (it may be non-linear). Voltage decay may also depend on other parameters, such as diode base width junction capacitance and parallel resistance. The former allows us to determine highest level lifet ime τ_{HL} (Carrier high injection), while latter permits us to extract low level life time τ_{LL} (Carrier low injection) [11]. In this work, two different types of silicon substrates have been used to synthesize (PS/c-Si) heterojunction by electrochemical etching with different etching times under dark and light conditions. The second objective of this paper is to estimate carrier life time of heterojunction as a function of preparation conditions.

2. Experimental details

Porous silicon layers were synthesised on both one side mirror- like monocrystalline *n*-and *p*-type (111) silicon wafers, with resistivity in range of 14–22 Ω cm for *p*-type

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and in range of 5–10 Ω cm for *n*-type. Samples were etched by using mixture of 40 % HF: 99.9 % Methanol (1:1) for 5 and 10 min with current density of 40 mA/cm^2 in dark for *p*-type and subjected to external illumination with a 30 mW diode laser 650 nm for *n*-type.A schematic diagram of electrochemical etching system is displayed in Fig. 1(a) and 1(b), we used same set-up presented in [12]. After electrochemical etching, samples were cleaned with methanol and distilled water. Metallization on pS also became another important area of interest, especially in Schottky diode structure. Success of pS in application areas depended on how challenges in seeking suitable metallization could be overcome [13]. Here ohmic contacts on both pS and bulk silicon were made by deposition of high purity Al films by using thermal resistive technique under vacuum pressure of 10^{-6} torr. After evaporation process, thickness of evaporated film on a glass substrate was measured using gravimetric method. Dark current–voltage measurements in forward and reverse directions of Al/PS/c-Si/Al heterojunction were carried out. Measurements of photocurrent of heterojunction were done under white light of different illumination power densities supplied by a halogen lamp with power of 150 W, which was connected to a Variac and calibrated by power meter. Open circuit voltage (V_{oc}) of heterojunction was investigated as function of light power. Life time measurement of photovoltaic porous devices was measured using OCVD technique. For this measurement a stroboscope and storage CRO (Philips 100 MHZ) were used. This magnitude could be determined from slope of voltage decay $\Delta V/\Delta t$ using Eq. (1). A steady-state excess carrier concentration was applied by a forward current flow through a diode. After an abrupt opening of the circuit at $t = 0$, recombination of excess carriers would take place and the diode's open voltage was monitored (as shown in Fig. 2). Initial voltage step at $t = 0$ was due to voltage drop in diode,which was observed when the current flow stoped [14].

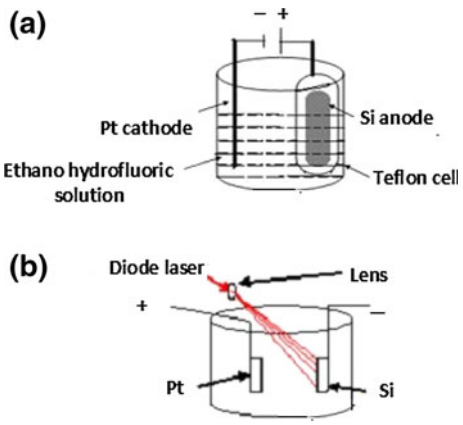

Fig. 1 (**a**) Schematic diagram of electrochemical anodization system (ECE) [15] and (**b**) schematic diagrams of photo electrochemical etching (PECE)

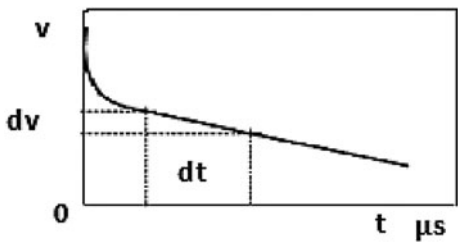

Fig. 2 Variation of voltage after opening the circuit (OCVD method) [10]

3. Results and discussion

Figure 3(a) and 3(b) show the morphology of pS. This confirms anodic dissolution of silicon surface leading to porous structure formation and variation of silicon surface colors indicate these surfaces are having different band gap and hence give different photoluminescence. Fig. 3(c) reveals the optical micrograph of pS surfaces formed at 40 mA/cm^2 etching current density for etching time of 10 min. This figure indicates a significant variation in microstructure between the mirror-like silicon surface and porous surface.

Figure 4 shows relation between open-circuit voltage (V_{oc}) and incident photon power of halogen lamp for *p*- and *n*-type heterojunctions prepared at different etching times. Both devices (Al/pS/p-Si/Al, Al/pS/n-Si/Al) show photovoltaic effect with similar V_{oc}. It observed that these heterojunctions have good linearity characteristics and saturation occurs after power density ≥5 mW/cm^2. Figures 5 and 6 show forward and reverse current–voltage characteristics of heterojunctions measured under dark and illumination with different light power densities respectively. The photocurrent is measured for light power densities of 1.2–20 mW/cm^2. The current starting at a low voltage corresponds to that of a typical thermionic emission. In linear region, thermionic emission and carrier velocity increases. When light power density is increased, the photocurrent is increases due to generation of electron–hole pairs. No soft breakdown has been noticed in the prepared heterojunctions at voltage <6 V. These results are in good agreement with those reported earlier [12]. OCVD shapes for prepared heterojunctions are shown in Figs. 7(a), 7(b) and 8(a), 8(b) for *n*- and *p*-type, respectively. Life time values obtained from Figs. 7 and 8 by using Eq. (1) under a condition of intermediate injection, where excess minority carrier concentration in base is higher than thermal-equilibrium minority carrier concentration but less than thermal equilibrium majority carrier concentration. These values are higher than those reported earlier [15]. Life time dependence on V_{oc} is exponential in broad terms [16]. The minority carriers life time decreases with increasing etching time for both of *n*- and *p*-type

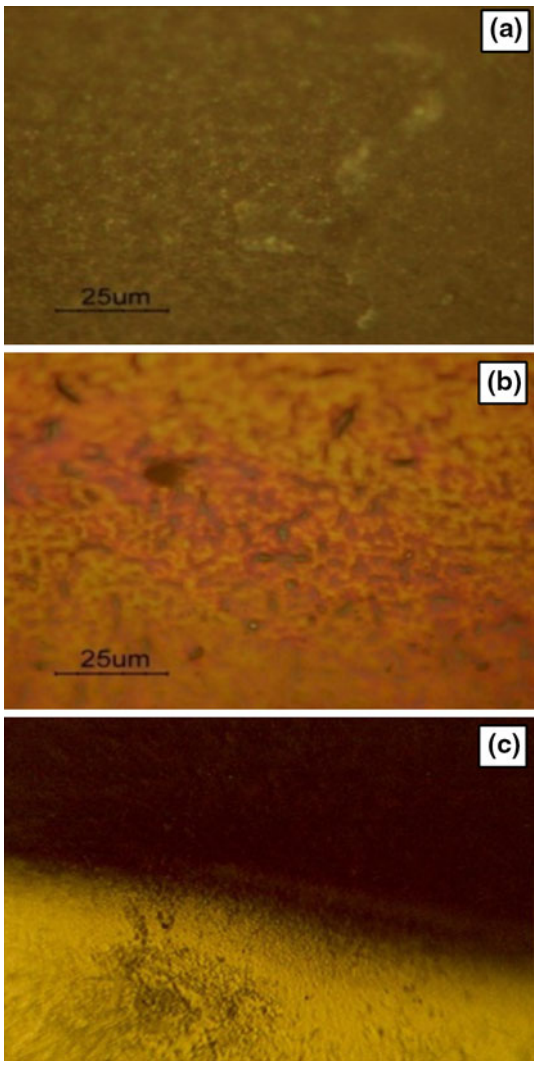

Fig. 3 (**a**) Optical micrograph of pS surface on n-Si formed at 40 mA/cm^2 etching current density (M = 1,000) (**b**) optical micrograph of pS surface on p-Si formed at 40 mA/cm^2 etching current density (M = 1,000), and (**c**) optical images of cross-sections of Porous silicon pS/Si –interface

heterojunctions. It means that probability of recombination decreases with increasing etching time leading to an increase of recombination centers which arise from point defects. Relation between porosity, thickness and etching current density leads to porous structure which reduces the recombination center, thus giving information about lower defect densities in the interface of heterojunctions. It has been found that the carrier life time in the structure of porous heterojunction is always non-uniformly distributed and the difference over large area may be considerable. Thus, this study confirms that OCVD method is very sensistive to structural defects [10]. Experimental results reveal that recombination center sites are produced either inside the bulk (substrate) or at surface/interface depending on heterojunction preparation conditions. The excess

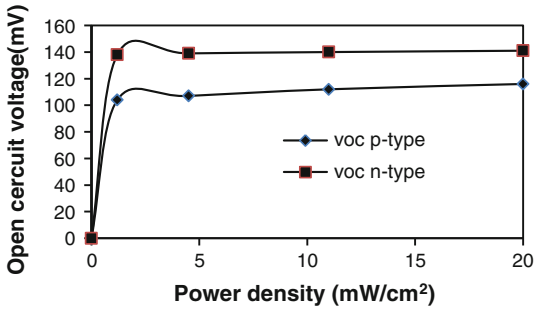

Fig. 4 Open circuit voltage as a function of the incident photo energy at 5 min etching for p- and n-type substrate

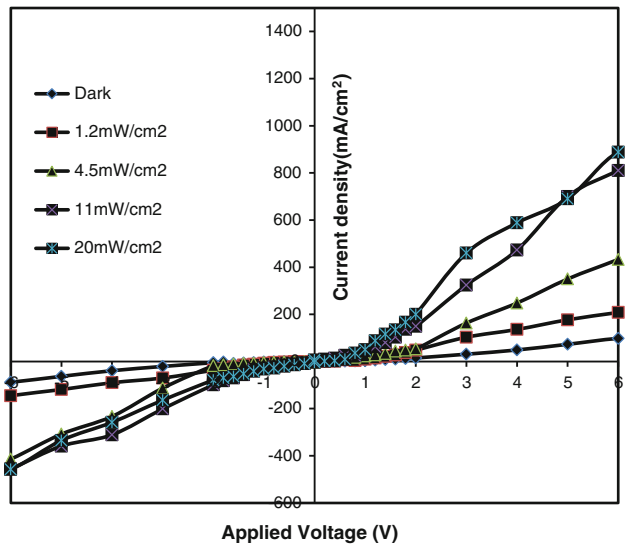

Fig. 5 Dark and Photo-current of pS/p-Si heterojunction as a function of forward and reverse bias illuminated for different power density at 10 min etching time, 40 mA/cm^2

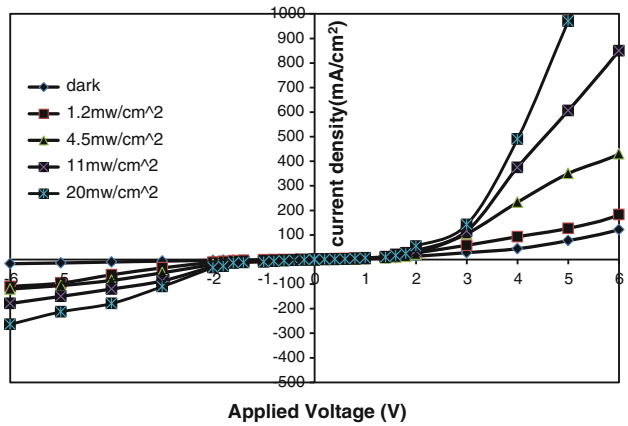

Fig. 6 Dark and Photo-current of pS/n-Si heterojunction as a function of forward and reverse bias illuminated for different power density at 10 min etching time, 40 mA/cm^2

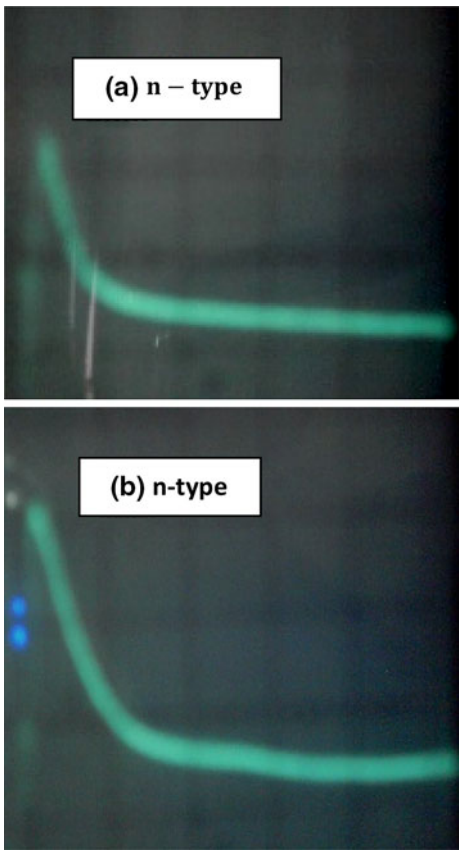

Fig. 7 (**a**) Photo-Induced Open-Circuit Voltage Decay Photograph for different etching current density at 5 etching time ($\tau = 208$ μs, J = 40 mA/cm^2, Hor.50 μs/div, Ver.10 mV/div) and (**b**) photo-Induced Open-Circuit Voltage Decay Photograph for different etching current density at 10 etching time ($\tau = 125$ μs, J = 40 mA/cm^2, Hor.50 μs/div)

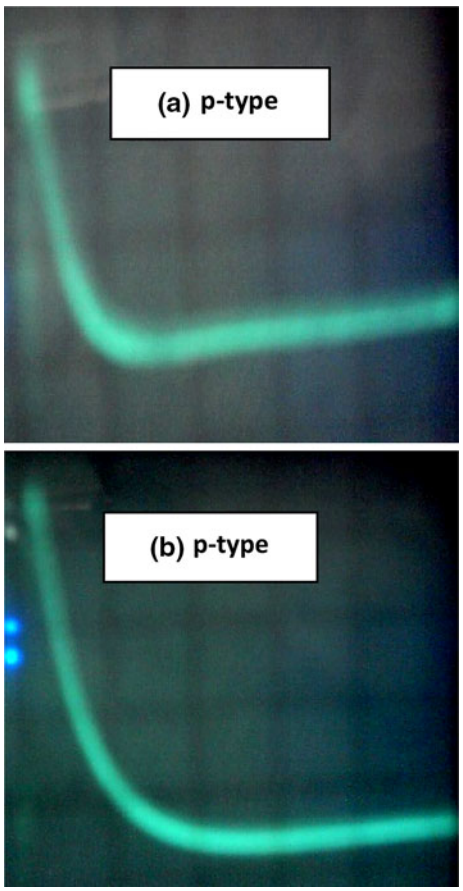

Fig. 8 (**a**) P Photo-Induced Open-Circuit Voltage Decay Photograph for different etching current density at 5 etching time ($\tau = 113$ μs, 40 mA/cm^2, Hor.50 μs/div, Ver.10 mV/div) and (**b**) photo-Induced Open-Circuit Voltage Decay Photograph for different etching current density at 10 etching time ($\tau = 83$ μs, 40 mA/cm^2, Hor.50 μs/div, Ver.10 mV/div)

carriers' life time measured by OCVD, provides a carrier effective life time bulk life time $\tau_{m,eff}$ depending on τ_m, bulk and surface life time $\tau_{m,surf}$ as shown in the following equation [17]:

$$\frac{1}{\tau_{m\ eff}} = \frac{1}{\tau_{m\ bulk}} + \frac{1}{\tau_{m\ surface}} \quad (2)$$

Accuracy of OCVD measurement depends on precession of oscilloscope, temperature measurement and noise. The total error of estimated lifetime is lower than 10 %. The diode works in on-state under a resistive load with a small parasitic inductance in series. With a sudden stop of current flow using fast external semiconductor switch, leaving the diode in an open circuit and forcing excess carrier removal by internal recombination and diffusion processes. This is electrically manifested on time decay of diode voltage drop, in which two linear slopes that correspond to the conditions of high or low injection are observed [11].

4. Conclusions

Optoelectronic properties and minority carrier life time of Al/pS/Si/Al heterojunctions are measured as a function of preparation conditions. The carrier lifetime decreases with increasing etching time for both *n*-and *p*-type heterojuctions. Highest value of minority carrier life time is obtained for heterojunction prepared on *n*-type substrate for 5 min and this value can be refered to an improvement in the bulk life time after creation of porous layer. Heterojunctions show good linearity characteristics and saturation occurs at a power density >5 mW/cm^2.

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